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EXAMINER	
AHMED, SAMIR ANWAR	

ART UNIT	PAPER NUMBER
2623	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/711,595	SHINOHARA, MAMORU	
	Examiner	Art Unit	
	Samir A. Ahmed	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's amendment filed on 3/08/04 has been entered and made of record.

2. Applicant has only labeled Figs. 4 and 5A as prior art. Applicant did not label Fig. 5B as prior art. The grounds for objection to Fig. 5B stated in paragraph 1 of the Office Action mailed on 2/17/04 paper number 10, are incorporated by reference herein.

3. Applicant did not amend Fig. 2 to show "the static electricity drawing wiring 401 protrudes from the fingerprint recognizing surface upwardly" as described in the specification on page 19, lines 14-18. The grounds for objection to Fig. 2 stated in paragraph 2 of the Office Action mailed on 2/17/04 paper number 10 are incorporated by reference herein.

4. In response to Applicant's amendment filed on 3/08/04 the objection to claims 1-10 is withdrawn.

5. In response to Applicant's amendment filed on 3/08/04 the rejection of claims 2, 8, 12, 18 under 35 U.S.C. 112, first paragraph is withdrawn.

6. Applicant has substantially amended independent claims 1, and 11 to traverse the prior art of record. Applicant's arguments filed 3/08/04 have been fully considered but they are moot in view of new grounds for rejection.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-20,are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Applicant's admitted prior art (Figs. 4, 5A, 5B) and Machida et al. (6,248,655).

As to claim 1, Applicant's admitted prior art discloses a semiconductor apparatus, comprising:

a substrate having a transistor (Fig. 5A, substrate 10, Fig. 5B transistor WL1);

a plurality of first capacitor electrodes secured to said substrate (Fig 5A electrodes 21(52)); and

an insulating film formed so as to cover said first electrodes (Fig. 5A, insulation film 30(53)). Applicant's admitted prior art does not disclose, a plurality of second electrodes secured to said substrate and electrically separated from said first electrodes, and the insulating film is between the first electrodes and second electrodes

Wherein, the first and second electrodes have a common bottom level and the plurality of second electrodes each have a top surface which is above a top surface of the first electrodes.

Machida discloses a conventional capacitive fingerprint sensor (similar to that discloses by Applicant's admitted prior art) where plurality of capacitive sensor electrodes 2406 are secured on a semiconductor substrate and covered by a passivation film 2407 of insulating material. The capacitive sensor is mounted together with an LSI (integrated circuit) chip on the substrate. However since the skin of the finger is used as an electrode, an LSI mounted on the substrate together with the sensor is susceptible to damage due to static electricity generated when the skin

touches the sensor (col. 2, lines 7-67, Figs 24, 25). Machida is solving this problem exits in the conventional prior art disclosed in both Applicants admitted prior art and Machida's back ground (col. 3, lines 8-12). This is the same problem that the instant invention is solving.

Machida discloses a capacitive fingerprint sensor as shown in Figs. 10, 11F, 12A-12C comprises a substrate 1001, a plurality of capacitive sensor electrodes 1005 (claimed first capacitor electrodes) secured to the substrate, a plurality of ground electrodes 1006 (claimed second electrodes) secured to the substrate and electrically separated from sensor electrodes 1005. A passivation film 1007 is formed to cover sensor electrodes 1005 and which is between sensor electrodes 1005 and ground electrodes 1006. the passivation film 1007 is made up of an insulating material (Fig. 10, col. 22, line 47-col. 23, line 14, Fig. 11F, col.24, lines 60-67, Figs. 12A-12C, col. 25, lines 1-17). As clearly shown by Figs 10, 11F, 12A, the sensor electrodes 1005 and the ground electrodes 1006 have a common bottom level and the ground electrodes 1006 each have a top surface which is above the top surface of sensor electrode 1005. One of ordinary skill in the art would recognize that the transistor mounted on the substrate together with the sensor in Applicant's admitted prior art finger print sensor is susceptible to damage due to static electricity generated when the skin touches the sensor. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use Machida's teachings to modify Applicant's admitted prior art fingerprint sensor by using ground electrodes (second electrodes) in the insulating film, the ground electrodes are separated from the sensor electrodes (first electrodes), have a common bottom level,

and the ground electrodes (second electrodes) have a top surface which is above the top surface of the sensor electrodes (first electrodes) in order to when the finger touches the ground electrodes the static electricity flows to the ground electrodes. This suppresses damage to other integrated circuit portions formed below the ground electrodes due to the static electricity (col. 24, lines 18-26) and to reliably perform stable, high sensitivity surface shape (fingerprint) detection without causing damage due to static electricity in sensing operation (col. 3, lines 8-12).

As to claim 2, Machida further discloses, wherein said top surface of the second electrodes is substantially equivalent to a top surface of said insulating film [Fig. 10 shows the top surface of passivation film 1007 is substantially equivalent to the top surface of the ground electrodes 1006].

As to claim 3, Machida further discloses, the passivation film 1007 (insulating film) is formed to cover the sensor electrodes 1005 (first electrodes). The upper portions of the ground electrodes 1006 (second electrodes) are exposed on the upper surface of the passivation film 1007 (Fig. 10, col. 22, lines 64-67, col. 24, lines 60-64). One of ordinary skill in the art would recognize from the nature of the problem to be solved, i.e., maintaining the upper portions of the ground electrodes (second electrodes) exposed on the upper surface of the passivation film (the insulating film) adjacent to the ground electrodes is only realized by either keeping the upper portions of the ground electrodes (second electrodes) at the same level of the upper surface of the passivation film (the insulating film) (i.e., same height) or keeping the upper portions of the ground electrodes (second electrodes) at a higher level than the upper surface of the

passivation film (the insulating film) (i.e., the ground electrode height is larger than the passivation film height).

As to claim 4, Machida further discloses, wherein said second electrodes are fixed to constant potential [the ground electrodes 1006 (second electrode) are connected to the ground (col. 23, lines 36-39), i.e. fixed to a zero potential (constant potential)].

As to claim 5, Machida further discloses, wherein a plurality of said first electrodes are arranged in a matrix form, and said second electrodes are disposed between said plurality of first electrodes (Fig. 1B, sensor electrodes 105 (first electrodes), support electrodes 106 (second electrodes), col. 23, lines 59-63, Fig. 12C, col. 27, lines 1-5, col. 28, lines 42-52, Fig. 5, items 10, 12, and 32).

As to claim 6, Machida further discloses, wherein a said second electrodes are arranged in a matrix form (col.27, lines 1-5, Fig. 12C, col. 28, lines 42-52).

As to claim 7, Applicant's admitted prior art further discloses, wherein at least one of said first electrodes are connected to a first terminal of said transistor [Fig. 5B, transistor WL1 is connected to electrode 21 (first electrode)], and a second terminal of said transistor is connected to a bit line and a capacitance element to which a potential is applied [Fig. 5B, second terminal of transistor WL1 is connected to capacitor CB and a potential Vcc is applied to the bit line BL1 (page 5, lines 9-14)].

As to claim 8, Machida further discloses, wherein said second electrode is fixed to a constant potential [the ground electrodes 1006 (second electrode) are connected to the ground (col. 23, lines 36-39), i.e. fixed to a zero potential (constant potential)].

As to claim 9, refer to claim 8 rejection.

As to claim 10, Machida further discloses, wherein said second electrodes are electrically connected to a pad electrode which is connected to a corresponding lead for taking a signal out [Fig. 1A, pad 102a, Fig. 10, col. 23, lines 7-14, col. 24, lines 18-26, lines 52 –59].

As to claim 11, refer to claim 1 rejection. Machida further discloses a semiconductor substrate (Fig. 10, item 1001, col. 23, lines 20-21

As to claim 12, refer to claim 2 rejection.

As to claim 13, refer to claim 3 rejection.

As to claim 14, refer to claim 4 rejection.

As to claim 15, refer to claim 5 rejection.

As to claim 16, refer to claim 6 rejection.

As to claim 17, refer to claim 7 rejection.

As to claim 18, refer to claim 8 rejection.

As to claim 19, refer to claim 9 rejection.

As to claim 20, refer to claim 10 rejection.

9. Claims 3, 13,are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Applicant's admitted prior art (Figs. 4, 5A, 5B) and Machida et al. (6,248,655) as applied to claim 1 and 11 above and further in view of Knapp (U.S. Patent 5,325,442).

As to claim 3, Machida further discloses, the passivation film 1007 (insulating film) is formed to cover the sensor electrodes 1005 (first electrodes). The upper portions

of the ground electrodes 1006 (second electrodes) are exposed on the upper surface of the passivation film 1007 (Fig. 10, col. 22, lines 64-67, col. 24, lines 60-64). Machida does not clearly disclose, wherein a distance between a top surface of said substrate and said top surface of the second electrodes is larger than a distance between the top surface of said substrate and the top surface of said insulating film.

Knapp discloses a capacitive fingerprint sensor that uses sensor electrodes (14) (first electrodes) and ground electrodes (53 or 54) (second electrodes) secured to a semiconductor substrate 30, the ground electrodes (second electrodes) are deposited on the surface of the insulating film 32, in order to improve the electrical contact of the ground electrodes to the finger surface (Figs. 7a, 7b, 8), i.e., distance between a top surface of said substrate and said top surface of the second electrodes is larger than a distance between the top surface of said substrate and the top surface of said insulating film. One of ordinary skill in the art would recognize that maintaining the top surface of the ground electrodes (second electrodes) at larger height than the sensor electrodes (first electrodes) would improve the electrical contact of the ground electrodes to the finger surface and insure the discharge of the static electricity on the fingertip to protect the integrated circuits of the fingerprint senor. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use Knapp's teachings to modify the combined fingerprint sensor of Applicant's admitted prior art and Machida by maintaining a distance between a top surface of said substrate and said top surface of the second electrodes is larger than a distance between the top surface of said substrate and the top surface of said insulating film in order to improve the electrical

contact of the ground electrodes to the finger surface and insure the discharge of the static electricity on the fingertip to protect the integrated circuits of the fingerprint senor.

As to claim 13, refer to claim 3 rejection.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samir A. Ahmed whose telephone number is 703-305-9870. The examiner can normally be reached on Mon-Fri 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on 703-308-6604. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SA

SAMIR AHMED
PRIMARY EXAMINER